(19) (11) Publication number: **62016289 A**

Generated Document.

PATENT ABSTRACTS OF JAPAN

(21) Application number: **60157413**

(22) Application date: **16.07.85**

(51) Intl. Cl.: **G11C 7/00** G11C 8/00

(30) Priority:

(43) Date of application publication: **24.01.87**

(84) Designated contracting states:

(71) Applicant: **NEC CORP**

(72) Inventor: **MIBUCHI MAKOTO**

(74) Representative:

(54) READ ONLY MEMORY

(57) Abstract:

PURPOSE: To unitedly input a chip selecting signal with an address signal and to decrease the number of terminals of ROM by sharing both terminals for selecting the address and the chip.

CONSTITUTION: At terminals I0WI7 of a case 1 of a ROM, address signals A17A16...A1A0 are impressed ranging to timings t0Wt2, and a part A17A16 of the address signal and chip selecting signals CS1WCS3 are impressed at the timing t2. Thus, the chip selecting signal can be unitedly inputted with the address signal, and the number of the terminals can be decreased by the sharing of the terminals.